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(54) **Name of Invention:** Semiconductor Device and its Method of Manufacture

(57) **Summary**

**Topic:** Providing a reliable semiconductor device, and its method of manufacture, that makes electrode film thickness sufficient and uniform in stack-cell capacitors, satisfies required performance and improves the degree of integration.

**Means of Resolution:** Semiconductor devices such as dynamic RAMs in which multiple stack-cell capacitors CAP are aligned in a row with prescribed spacing on $P^-$ silicon substrate 1, with each made up of a nearly vertical tubular lower electrode (cylindrical polysilicon layer 96), a dielectric film (silicon nitride film 77) and an upper electrode (plate electrode 78 of polysilicon), with the afore-noted spacing in the direction of their alignment being smaller than the inner diameter of the afore-noted lower electrode.

**Scope of patent Application**

**Application Item 1** A semiconductor device in which multiple stack-cell capacitors are positioned in a row with prescribed spacing on a semiconductor substrate, and each consisting of a nearly vertical tube-shaped lower electrode, a dielectric film and an upper electrode, and with the afore-noted spacing at which they are placed being smaller than the inner diameter of the afore-noted lower electrodes.

**Application Item 2** The semiconductor device described in Application item 1, in which the inner surface of the lower electrode is a nearly vertical surface from its lower end to its upper end and its outer surface is nearly vertical from

the lower end part way to its top, but from there to the upper end its film becomes thinner.

**Application Item 3** The semiconductor device described in Application Item 1 or 2, in which the lower electrode is connected to the memory cell's diffusion region via a contact hole.

**Application Item 4** A method of manufacturing a semiconductor device which—when manufacturing the semiconductor device with multiple stack-cell capacitors situated in a row with prescribed spacing on a semiconductor substrate, and with each consisting of a nearly vertical tube-shaped lower electrode, a dielectric film and an upper electrode, and with the afore-noted spacing at which they are placed being smaller than the inner diameter of the afore-noted lower electrodes—has

- A process to form a spacer material on the semiconductor substrate in order to set the shape of the afore-noted stack-cell capacitors, *
- A process to form multiple masks on the afore-noted, situating them with specified spacing and to make the afore-noted spacing at which they are set smaller than the masks' diameter and thickness,
- A process to etch the afore-noted spacers using the afore-noted masks, to separate the spacer material into multiple spacers by selective removal of the afore-noted spacer material and to designate the inner diameter of the afore-noted lower electrodes with the material of each spacer,
- A process to apply the afore-noted lower electrodes' configuring material layer to the surface of the afore-noted spacer material,
- A process to etch the afore-noted configuring material layer, but leave that layer on the side surfaces of the afore-noted spacer material,
- A process to form the afore-noted lower electrode by removing the afore-noted spacer material,
- A process to form the afore-noted dielectric film at least on the surface of the afore-noted lower electrode and
- A process to form the afore-noted upper electrode at least on the surface of the afore-noted dielectric film.

*[Bullets added by translator.]

**Application Item 5** The manufacturing method described in Application item 4, which makes the spacing for the mask material 1/2 to $1/10^{th}$ or less of its thickness.

**Application Item 6** The manufacturing method described in Application Item 4 which makes the spaces between the mask material 1/2 to $1/10^{th}$ or less of the combined thickness of the material plus the thickness of the material etched immediately under the region of the material.

**Application Item 7** The manufacturing method described in one of Application Items 4~6, in which one etches the spacer material using an etching gas favoring slight anisotropy in the etched laminate.

**Application Item 8** The manufacturing method described in one of Application items 4~7, in which the lower electrode is connected to the memory cell's diffusion region via a contact hole.

**Application Item 9** A semiconductor device equipped with stack-cell capacitors on a semiconductor substrate, in which these tubular stacked capacitors consist of a lower electrode in an inverted base shape in cross section, a dielectric film and an upper electrode.

**Application Item 10** The semiconductor device described in Application Item 9, in which multiple stack-cell capacitors on a semiconductor substrate are located in a row with prescribed spacing, each consisting of a lower electrode with an inverted base shaped cross section, a dielectric film and upper electrode, and having their spacing on the axis in which they are aligned smaller than the outer diameter of their lower electrode.

**Application Item 11** The semiconductor device described in either Application item 9 or 10, in which the outer surfaces of the lower electrodes are nearly flat from bottom to top, while their inner surfaces are nearly flat from the bottom to a position part way to the top but become thinner from that point up to the top.

**Application Item 12** The semiconductor device described in any one of Application Items 9~11, in which the lower electrode is connected to the memory cell's diffusion region via a contact hole.

**Application Item 13** In manufacturing a semiconductor device wherein stack-cell capacitors are installed on a semiconductor substrate and consist of a tubular lower electrode with a cross section having an inverted base shape, a dielectric film and an upper electrode, a method of fabricating semiconductor devices, which has -

- A process to form spacer material on the afore-noted semiconductor substrate so as to designate the afore-noted shape of the stack-cell capacitors,
- A process to make a first mask on the afore-noted spacer material,
- A process to etch the afore-noted spacer material using the afore-noted first mask material, to selectively remove the afore-noted spacer material immediately under the non-masked regions and set the outer diameter of the afore-noted lower electrode,
- A process to make at least the configuring material layer of the afore-noted lower electrode adhere to the surface of the afore-noted spacer material,
- A process to fill in the region from which the afore-noted spacer material was removed with a second mask material up to a height just below the upper surface of this spacer material,
- A process to etch-back the afore-noted configuring material layer exposed at the upper surface of the afore-noted spacer material and nearby,
- A process to remove the afore-noted second mask material and leave the afore-noted configuring material layer on the side surfaces of the afore-noted spacer material,
- A process to form the afore-noted dielectric film at least on the surface of the afore-noted lower electrode and
- A process to form the afore-noted upper electrode at least on the surface of the afore-noted lower electrode.

**Application Item 14** In fabricating the semiconductor device on which multiple stack-cell capacitors are aligned with specified spacing on a semiconductor substrate and each is made up with a tubular lower electrode having the cross section of an inverted base, a dielectric film and an upper electrode and the afore-noted spacing is smaller than the outer diameter of the afore-noted lower electrode, the method of fabrication described in Application Item 13, which has -

- A process to form spacer material on the afore-noted semiconductor substrate so as to provide the afore-noted shape of the stack-cell capacitors,
- A process to form multiple first mask materials on the afore-noted spacer material so as to be aligned with specified spacing, making the afore-noted spacing larger than the diameter and thickness of the afore-noted first mask material,
- A process to etch the afore-noted spacer material using the afore-noted mask material, to selectively remove the afore-noted spacer material directly under the regions of the afore-noted spaces, individually separating them and to set the outer diameter of the afore-noted lower electrode with each spacer,
- A process to apply the configuring material layer of the afore-noted lower electrodes adhere at least to the surface of the afore-noted spacer material,
- A process to fill in between the afore-noted multiple separated spacers with a second mask material to a height below the top surface of these spacers,
- A process to etch the afore-noted configuring material layer where it is exposed at the upper surface of the afore-noted spacers and near them,
- A process to remove the afore-noted second mask material, leaving the afore-noted configuring material layer on the side surfaces of the afore-noted spacer-material,
- A process to remove the afore-noted spacer material and so form the afore-noted lower electrode,
- A process to form the afore-noted dielectric film at least on the outer surface of the afore-noted lower electrode and
- A process to form the afore-noted upper electrode on the upper surface of the afore-noted dielectric film.

**Application item 15** The manufacturing method described in Application Item 12 or 14, which makes the diameter of the spacers' non-masked region or the spacing of the first mask material 1~10 times this first mask material's thickness.

**Application Item 16** The fabricating method described in Application Items 13 or 14, in which the diameter of the first spacer material's spacing is made 1~10 times the total thickness of this first mask material plus either the thickness of the above-noted non-masked region or the thickness of

the etched material in the region directly below the above-noted spaces.

**Application Item 17** The fabrication method described in any one of Application Items 14~16, in which the lower electrode is connected to the memory cell's diffusion region via a contact hole.

**Application Item 18** In fabricating a semiconductor device in which stack-cell capacitors are installed on a semiconductor substrate and these stack-cell capacitors are made up of a tubular lower electrode, a dielectric film and an upper electrode, a method of manufacturing a semiconductor device which has -

- A process to make spacer material for fixing the shape of the afore-noted stack-cell capacitors on the afore-noted semiconductor substrate,
- A process to make mask material on the afore-noted spacer material,
- A process to etch the afore-noted spacer material using the afore-noted mask material in selectively removing the afore-noted spacer material directly under the non-masked region and in setting the diameter of the afore-noted lower electrode,
- A process to apply a configuring material layer of the afore-noted lower electrode at least to the surface of the afore-noted spacer material,
- A process to etch the afore-noted configuring material layer under etching conditions that lower the etching selectivity for oxides and that have isotropic etching ingredients, and to leave the afore-noted configuring material layer on the sides of the afore-noted spacer material under conditions that keep valleys from forming on the top end of the afore-noted configuring material as a result of this etching,
- A process to remove the afore-noted spacer material to form the afore-noted lower electrode,
- A process to form the afore-noted dielectric film at least on the surface of the afore-noted lower electrode and
- A process to form the afore-noted upper electrode at least on the upper surface of the afore-noted dielectric film.

**Application Item 19** In manufacturing a semiconductor device on which stack-cell capacitors are installed on a

semiconductor substrate and which these stack-cell capacitors consist of a tubular lower electrode, a dielectric film and an upper electrode, a method of fabricating a semiconductor device that has -

- A process to make spacer material for fixing the shape of the afore-noted stack-cell capacitors on the afore-noted semiconductor substrate,
- A process to make mask material on the afore-noted spacer material,
- A process to etch the afore-noted spacer material using the afore-noted mask material in selectively removing the afore-noted spacer material directly under the non-masked region and in setting the diameter of the afore-noted lower electrode,
- A process to apply a configuring material layer of the afore-noted lower electrode at least to the surface of the afore-noted spacer material,
- A process to etch the afore-noted configuring material layer, leaving the afore-noted configuring material layer on the sides of the afore-noted spacer material,
- A process to do isotropic etching after the afore-noted etching on the upper end of the afore-noted configuring material layer so as to remove valleys formed by this etching,
- A process to remove the afore-noted spacer material to form the afore-noted lower electrode,
- A process to form the afore-noted dielectric film at least on the surface of the afore-noted lower electrode and
- A process to form the afore-noted upper electrode at least on the upper surface of the afore-noted dielectric film.

**Application item 20** The manufacturing process described in Application Item 18 or 19, which fabricates the semiconductor device described in any one of Application Items 1~3 and 9~12.

**Detailed Explanation of Invention**

**0001 Technical Field to Which the Invention belongs** This invention is one relating to a semiconductor device (in particular a round tubular dynamic RAM [random access memory of the stacked type] and its method of manufacture.

**0002 Usual Technology** Usually, semiconductor integrated circuit devices such as dynamic RAMs having stacked-structure elements in the memory area, such as stack-cell capacitors made in a round shape to increase capacity, are fabricated through processes such as those shown in Figures 28-33.

**0003** As shown in Figure 28, for this memory cell part $N^+$ semiconductor regions 3 (source region) and 4 (drain region) are formed by the self-aligning method with word line WL as a mask, installing an element region on $P^-$ silicon substrate 1 with field silicon oxide film 2 formed by the LOCOS method (local oxidation of silicon). On this are formed polysilicon word line WL with silicon nitride sidewall 60 on it, as well as insulating film 6 formed by CVD (chemical vapor deposition).

**0004** Contact hole 49 is opened in dielectric film 6 through to $N^+$ drain region 4, and bit line BL is made on that. Insulating layer 61 protects the upper surface of bit line BL, and sidewalls 62 are installed on its side surfaces. Contact hole 10 is made in insulating layer 6 on source region 3 and part of insulating layer 70. Polysilicon layer 11 is applied by CVD, making up part of the capacitor's lower electrode (storage node) so as to connect with this contact hole 10 and source region 3.

**0005** On this polysilicon layer 11 one uses CVD to form oxide insulating layer 71 of silicate glass that will be a support for a spacer designating the shape of a polysilicon lower electrode) when making the tubular stack-cell capacitor to be discussed later. And one forms photo-resist mask 72 in a prescribed pattern for etching this insulating layer 71 into the shape of a spacer.

**0006** Then, as shown in Figure 29, one uses mask 72 to dry-etch insulating layer 71, selectively removing silicate glass layer 71 from immediately under non-masked region 73. For the etchant in this dry etching, one uses a mixture of $CF_4$, $CHF_3$ and Ar. However, etching vertically as shown in the figure is difficult, while etching on the inverted base shape of slope 74 is easier.

**0007** The reason for this is thought to be that when the dielectric surface under non-masked region 73 is etched a laminate 75 from the etchant gas (especially that created by $CHF_3$) adheres to the slope and coats the sloped surface before it is etched in a vertical direction, so that this condition

creates a virtual line in the direction of insulating layer 71's thickness, causing a masking effect for dry etching. This laminate 75 arises on the sides of insulating layer 71 remaining in the spacer shape from the dry etching; but for simplification it is omitted in the following figure.

**0008** Now, as shown in Figure 30, on all surfaces one uses CVD to form polysilicon layer 76 that will become the lower electrode of the capacitor, and then—as shown in Figure 31—generally etches polysilicon layer 76 from the location of the broken line and goes on also to etch underlying polysilicon layer 11, leaving polysilicon layer 76 on the sides of spacer material 71. For this etch-back, one uses a mixture of chlorine and oxygen for their superior anisotropic traits. Since the sides of spacer 71 are sloped as noted above, as the etching gas is used perpendicular to the substrate on polysilicon layer 76's sloped surfaces (i.e., at right angles to substrate 1) it will be etched in the direction of its thickness, too.

**0009** As a result, polysilicon layer 76, which should remain thick at the broken-line position on spacer 71's side surfaces, become thinned. This will increase its electrical resistance as the capacitor's lower electrode, which is not desirable.

**0010** Now spacer material 71, which supports polysilicon layer 76 at the sides, is removed by wet etching or by dry etching with $CF_4/CHF_3/Ar$ as the etchant gases, as shown in Figure 32, thus forming tubular lower electrode 76 of polysilicon with a base shape connected to substrate 1's $N^+$ region 3.

**0011** Next, as shown in Figure 33, one does CVD on the whole surface to laminate highly dielectric film 77 of silicon nitride and the capacitor's upper electrode 78 (plate electrode) of polysilicon to finish fabricating memory cell MC' with a COB (Cell Over Bitline) structure having multiple separated stack-cell capacitors.

**0012** As we have noted above, with such a usual fabricating process, polysilicon layer 76 shown in Figure 31 easily becomes thinned after etching because spacer 71's sides become sloped due to the patterning shown in Figure 29; and that weakens its capacity as an electrode.

**0013** To avoid this problem then, one may conceive of making polysilicon layer 76 thicker, as shown in Figure 34, so as to leave adequate thickness on spacer 71's sloped surfaces with the etch-back shown in Figure 35.

**0014** However, that will also make polysilicon 76 thick where it adheres between the adjoining spacer materials 71-71, so that after an etch-back polysilicon layer 76 will remain between spacer materials 71-71 or else underlying polysilicon layer 11 somehow will not be etched. As a result, even when the capacitors are formed through the processes of Figures 32 and 33, conductance will occur between adjoining capacitors through their lower electrodes 76 and 11, making then unable to function.

**0015** In such case, it thus becomes necessary to make the distance between spacers 71-71 wide enough keep the adhering thickness of polysilicon film 76 between them from becoming too great. Yet, that increases the spacing between adjoining capacitors and does not meet the needs for higher integration and density.

**0016** Also, at the time of the above-noted polysilicon layer 76's etch-back, we found that valleys easily form in the remaining polysilicon layer 76.

**0017** That is, as shown in Figure 36(B), when polysilicon is etched-back from the condition shown in the enlargement in Figure 36(A), at the inner top edge of polysilicon layer 76 (the part in contact with spacer material 71) a polymer-like laminate 79 from the reaction of the etchant gases with the polysilicon has created a valley, while at the top outer edge of polysilicon layer 76 a natural oxide film 80 has already formed, and these remain as an unetched valley.

**0018** If dielectric film 77 and polysilicon upper electrode 78 are formed with such a valley remaining as shown in Figure 36(C), stresses will be added at the valley part, especially at dielectric film 77; and pinholes will form in that film or localized film thinning will arise (the part indicated by 81 in the figure). With such defects present, the dielectric film's insulation will fail or its voltage resistance will decrease. That means the memory cell's capacitor cannot store a charge normally and the memory cell cannot function.

**0019 Matters the Invention Seeks to Resolve** The purpose of this invention is to provide a semiconductor device of good

reliability and its method of manufacture which, in stack-cell capacitors, can make electrode film thicknesses that are adequate and uniform, improve the degree of integration and will definitely operate normally.

**0020 Means to Resolve the Problems** That is, this invention is one that relates to a semiconductor device made up of a semiconductor substrate (e.g., the later described $P^-$type silicon substrate 1), on which multiple stack-cell capacitors (e.g., the later described stack-cell capacitors CAP) are arrayed in a row with prescribed spacing, a crown-shaped lower electrode (e.g., the later described tubular polysilicon layer 96), a dielectric film (e.g., the later described silicon nitride film 77) and an upper electrode (e.g., the later described silicon plate electrode 78). Also, it is a semiconductor device in which the afore-noted spacing along their alignment is less than the inner diameter of the aforementioned lower electrode. This will hereafter be called the main invention's first invention.

**0021** With the semiconductor device of this first invention, spaces between the stack-cell capacitors are smaller than the diameter of the lower electrodes, making spaces between adjoining capacitors narrow. So, one can improve the integration. Also, that makes it difficult for etchants—the cause of the laminate formation—to invade the above-noted spaces corresponding to the non-masked region of the mask used in patterning the spacer material that sets the shape of the lower electrode during fabrication, so that one can adequately preserve the thickness of the capacitors' lower electrodes after the etch-back and so keep its vertical shape.

**0022** To fabricate the semiconductor device of this first invention, it is desirable to carry out a manufacturing process that has –

- A process to form on above-noted semiconductor substrate the spacer material (such as the later-described silicate glass layer 91) for providing the shape of the afore-noted stack-cell capacitors,
- A process to form a row of multiple mask materials on the afore-noted spacer material (such as the later-described photo resist mask 92) with prescribed spacing, in this instance making the afore-noted spacing smaller than the afore-noted mask material's inner diameter or thickness,
- A process that etches the afore-noted spacer material using the afore-noted spacer material to selectively

remove the afore-noted spacer material from the region directly under the regions of the afore-noted spaces to separate them individually, and that designates at least the inner diameter of the afore-noted lower electrode,

- A process that coats at least the surface of the afore-noted spacer material with a configuring material layer of the afore-noted lower electrode,
- A process that etches the afore-noted configuring material layer while leaving it on the sides of the afore-noted spacer material,
- A process that removes the afore-noted spacer material to form the afore-noted lower electrode,
- A process that forms a dielectric film at least on the surface of the afore-noted lower electrode and
- A process that at least forms the afore-noted upper electrode on the surface of the afore-noted dielectric film.

This hereafter is called the second invention of this invention.

**0023** In the fabrication method of this second invention the spacer material's etching-mask spacing is made less than its diameter and thickness, making it difficult during the etching (patterning) of the spacer material for the etchant to seep into the above-noted spaces. That allows vertical anisotropic etching to occur sufficiently. Due to that, the sides of the spacer material have good perpendicularity. That can prevent lateral etching during etch-back of the lower capacitor electrode's configuring material layer and can sustain its thickness.

**0024** As a result, there is no need to make the lower electrode's configuring material layer thick in advance to prevent the thinning previously described; and since one can make the spacing between capacitors as narrow as possible, one can work out the device's high density and improve its degree of integration.

**0025** Also, the main invention is one providing semiconductor devices on which stack-cell capacitors are installed on semiconductor substrates, with these stack-cell capacitors made up of tubular lower electrodes with an inverted-base shaped cross section, dielectric films and upper electrodes. Below this will be called this invention's third invention.

**0026** The semiconductor device of this third invention makes use of the fact that the lower electrodes of the stack-cell capacitors have a cross-sectional shape of inverted bases and that during etching of the previously described spacer material a slope is created on the inverted base shape and makes use of the spacer material corresponding to the spacing between adjoining lower electrodes. At the same time, by installing the lower electrode on the unmasked region from which the spacer material is to be removed, one gets a lower electrode that is an inverted base in cross section. So, by making the lower electrode this shape, one can make the space narrow between adjoining lower electrodes, enabling one to make the device higher density and more integrated.

**0027** To fabricate the semiconductor device of this third invention, it is desirable to do a fabrication method that has –

- A process to form on above-noted semiconductor substrate the spacer material to provide the shape of the afore-noted stack-cell capacitors,
- A process to form a first masking material (such as the later-described photo resist mask 102),
- A process to etch the afore-noted spacer material using the afore-noted first mask material to selectively remove the afore-noted spacer material from the region directly under the non-masked regions and set the outer diameter of the afore-noted lower electrode,
- A process to coat at least the surface of the afore-noted spacer material with a configuring material layer of the afore-noted lower electrode,
- A process to fill–up to a height below the upper surface of that spacer material–the region where the afore-noted spacer material was removed with a second spacing material (such as the later-described photo resist 101),
- A process to etch the upper surface of the afore-mentioned spacer material and the afore-noted configuring material layer that is exposed nearby,
- A process to remove the afore-noted second masking material, leaving the afore-mentioned configuring material layer on the sides of the afore-noted spacer material,
- A process to remove the afore-noted spacer material to form the afore-noted lower electrodes,
- A process to form the afore-noted dielectric film at least on the surface of the afore-noted lower electrode and

- A process to form the afore-noted upper electrode at least on the surface of the afore-noted dielectric film.

Hereafter, this will be called the fourth invention of the main invention.

**0028** With the fabrication method of this fourth invention, the spacer material's sides are sloped by adhesion of a laminate after the etching because the spacer material is etched via the unmasked region of the above-noted first masking material when forming the inverted base shape of the lower electrode in the above-noted third invention. RECHECK But, the lower electrode's adhering configuring material layer here is protected up to the upper surface of the spacer material by the second mask material and so is not etched. That means that the lower electrode remaining is adequately thick and so provides an inverted base shape matching the above-noted spacer material's sloped surfaces. That makes it possible for one to make the spacing between lower electrodes (i.e., the etched part of the above-noted spacer material) small and so to make the capacitor high density and highly integrated.

**0029** Also, the main invention is one that provides a method for manufacturing semiconductor devices, which—in fabricating a semiconductor device on which stack-cell capacitors installed on a semiconductor substrate and are made of a tubular lower electrode, a dielectric film and upper electrode —has:

- A process to form a spacer material on the above-noted semiconductor substrate to set the shape pf the above-noted stack-type capacitors,
- A process to form a mask material on the above-noted spacer material,
- A process to etch the above-noted spacer material, using the afore-noted mask material, selectively removing the afore-noted spacer material directly under the non-masked region to establish the diameter of the afore-noted lower electrode,
- A process to apply a configuring material layer for the afore-noted lower electrode at least on the upper surface of above-noted spacer material,
- A process to etch the lower electrode's configuring layer material under conditions that reduce the selective etching ratio for oxide and so has an isotropic etching component, and to leave the afore-noted configuring

material layer on the sides of the afore-noted spacing material under conditions that prevent formation of a valley on the upper end of the afore-noted configuring material layer that this etching would create,

- A process to remove the afore-noted spacer material to form the afore-noted lower electrode,
- A process to form the afore-noted dielectric film at least on the outer surface of the afore-noted lower electrode and
- A process to form the afore-noted upper electrode at least on the afore-noted dielectric film.

Hereafter we will call this the fifth invention of the main invention.

**0030** Because, when etching the lower electrode's configuring material layer with the fabrication method of this fifth invention, we etch under conditions having an isotropic component and so lowering the relative etching ratio for oxides, we can etch-back so as not to create the natural oxides and polymers that tend to form on the outer and inner sides of the lower electrode's configuring material layer and can prevent formation of valleys without adding a process. So, we can readily form dielectric film on the lower electrode that has adequate thickness and good film qualities, avoiding insulating failures and improving voltage resistance to elevate its reliability.

**0031** Furthermore, in fabricating a semiconductor device in which stack-cell capacitors are installed on a semiconductor substrate by making up this stack-cell capacitors of a tubular lower electrode, dielectric film and upper electrode, this invention is one that also provides a fabrication method for the semiconductor that has –

- A process to form on the afore-noted semiconductor substrate a spacer material for setting the shape of the afore-noted stack-cell capacitors,
- A process to form a mask material on the afore-noted spacer material,
- A process to etch the afore-noted spacer material using the afore-noted mask material and so selectively remove the afore-noted spacer material from directly under the non-masked region,
- A process to set the diameter of the afore-noted lower electrodes,

- A process to apply a configuring material layer of the afore-noted lower electrode at least on the outer surface of the afore-noted spacer material, a process to etch the afore-noted configuring material layer but leave it on the sides of the afore-noted spacer material,
- A process, after the above-noted etching, to do isotropic etching to remove valleys formed by the afore-noted etching on the upper end of the afore-noted configuring material layer,
- A process to remove the afore-noted spacer material and so form the afore-noted lower electrodes,
- A process to form the afore-noted dielectric film on the outer surface of the afore-noted lower electrodes and
- A process to form the afore-noted upper electrodes on the outer surface of the afore-noted dielectric film. Hereafter we will call this the sixth invention of the main invention.

**0032** With the fabrication method of this sixth invention, as contrasted to the above-noted fifth invention, one etches the configuring material layer of the lower electrodes to remove the valleys on top by isotropic etching; but it can yield the same effects in being able to form lower electrodes without valleys and sustain the thickness and quality of the dielectric film. Also, even though it adds a process to remove the valleys, this can be easily done by sending it to another treatment chamber with the vacuum intact.

**0033 Format for Doing This Invention** In the above-noted first invention of the main invention, the inner surface of the lower electrodes is nearly perpendicular from its lower end to its upper end, while the outer surface is nearly perpendicular from its lower end most of the way to its upper end, as the film may thin from that point along the way to the afore-noted upper end.

**0034** Also, the lower electrode may be connected to the memory cell's diffusion region via a contact hole.

**0035** Or, one may make the spacing of the mask material from 1/2 to $1/10^{th}$ the total of its thickness plus the thickness of the etched material directly under the region of the above-noted spacing.

**0037** Again, one may etch the spacing material using an etching gas with good anisotropic traits yielding few etching laminates.

**0038** Or one may make the lower electrode contact the diffusion layer of the memory cell via a contact hole.

**0039** In the above-noted three inventions of the main invention multiple stack-cell capacitors are arranged with prescribed spacing on a semiconductor substrate, each of them made up of an inverted-base shaped, tubular lower electrode, a dielectric film and upper electrode. The afore-noted spacing on the axis of their alignment is best if it is less than the outer diameter of the afore-noted lower electrodes.

**0040** Also, the outer surface of he lower electrodes is nearly flat from its lower to its upper end; and their inner surface may be nearly flat from its lower end almost to its upper end, where the film becomes thin.

**0041** Again, the lower electrode may be connected to the memory cell's diffusion region via a contact hole.

**0042** In the fourth invention of the main invention, when fabricating a semiconductor device in which multiple stack-cell capacitors are installed on a semiconductor substrate with prescribed spacing and these stack-cell capacitors consist of an inverted-base shaped tubular lower electrode, a dielectric film and upper electrode, and in which the afore-noted spacing on their axis of alignment is smaller than the outer diameter of the afore-noted lower electrodes, one may make the fabrication method one that has -

- A process to form spacer material for designating the shape of the afore-noted stack-cell capacitors on the afore-noted semiconductor substrate,
- A process to form multiple 1$^{st}$ masks with prescribed spacing on the afore-noted spacer material such that the afore-noted spacing in this case is larger than the diameter and thickness of the afore-noted 1st masks,
- A process to etch the afore-noted spacer material using the afore-noted 1$^{st}$ mask material, selectively removing that material directly under the region of the afore-noted spaces to separate them and set the outer diameter of the afore-noted lower electrodes with each spacer material,

- A process to apply a configuring material layer for the afore-noted lower electrode at least on the outer surface of the afore-noted spacer material,
- A process to fill the gaps between the afore-noted multiple separated spaces with a 2nd mask material to a height below the upper surface of these spacers,
- A process to etch-back the afore-noted configuring material layer that is exposed atop and near the afore-noted spacer material,
- A process to remove the afore-noted 2nd mask material, leaving the afore-noted configuring material layer on the side surfaces of the afore-noted spacer material,
- A process to remove the afore-noted spacer material and form the afore-noted lower electrodes,
- A process to form the afore-noted dielectric film at least on the outer surfaces of the afore-noted lower electrodes and
- A process to form the afore-noted upper electrodes at least on the outer surfaces of the afore-noted dielectric film.

**0043** Again, it is better to make the diameter of the spacer material's unmasked region or the spacing of the 1st mask material equal to, or up to 10 times the thickness of this 1st mask material.

**0044** Or, one may make the diameter of the spacer material's unmasked region or spacing of this 1st mask material equal to, or up to ten times the total thickness of this 1st mask material plus the thickness of the etched material immediately under the region of the afore-noted spacing.

**0045** Also, it is best to connect the lower electrode to the memory cell's diffusion region via a contact hole.

**0046** The above-described fifth and sixth inventions of the main invention are best done with the semiconductor device fabricating method discussed as modes for doing the above-noted first and third inventions.

**0047 Application Examples** We will explain examples of applying this invention below.

**0048** Figures 1~17 show the first application example of applying this invention to a dynamic RAM.

**0049** To explain the dynamic RAM from this application example along with its fabricating processes, first—as shown in Figure 1—one installs an element region with $SiO_2$ field film 2 formed by the LOCOS method on $P^-$ silicon substrate 1 in the memory cell area, then forms gate oxide film 5 in this element region, uses CVD to form polysilicon word line WL on this with sidewall 60 of silicon nitride and $SiO_2$ dielectric layer 6, and then uses the self-aligning mode with this word line WL as a mask to form $N^+$ semiconductor regions 3 (source region) and 4 (drain region).

**0050** In insulating layer 6 one opens contact hole 49 through to $N^+$ drain region 4 and forms the adhering bit line BL. The upper surface of bit line BL is protected by insulating layer 61 and silicon nitride sidewall 62 is installed on its sides.

**0051** Next, as shown in Figure 2, one uses CVD to apply insulating layer 70 of $SiO_2$ or the like (including a layer of phosphor-silicate glass) on the entire surface. Then, as shown in Figure 3, one forms contact hole 10 in dielectric layer 6 on source region 3 and part of 70.

**0052** Now, as shown in Figure 4, one uses CVD to apply polysilicon layer 11, for example 1000Å thick, which will become part of the capacitor lower electrode (the storage node) so that it connects with source region 3, including contact hole 10.

**0053** Then, as shown in Figure 5, on polysilicon layer 11 one uses CVD to install, for instance 5000Å thick, oxide insulating layer 91 that will become a support (or a spacer for setting the shape of the polysilicon lower electrodes) when forming the later-described tubular (crown-shaped) polysilicon lower electrode of the tubular stack-cell capacitors. This silicate-glass insulating layer 91 is made of a non-doped silicate glass with no impurities. (However, depending on the type of impurity and its concentration, one may dope it with an impurity.)

**0054** As shown in Figure 6, one next forms in a prescribed pattern a photo-resist mask 92 for etching insulating layer 91 in the shape of spacers—i.e., multiple separate round patterns. For this mask 92, one makes the diameter of each mask $W_1$, the spacing between each mask $W_2$ and the thickness H, and then can make it with $W_2$ = 0.2μm and H = about 2.0μm. It is desirable that one make the aspect ratios $2W_2 \leq W_1 \leq 10W_2$ and $W_2/H \leq 1/2$ (and also $1/10 \leq W_2/H \leq 1/2$). For instance, it is

best to make $W_1$ = 0.6~1.2m, $W_2$ = 0.2~0.3m, and for $W_2/H$ to be 0.3.

**0055** Next, as shown in Figure 7, one uses mask 92 in dry-etching insulating layer 91 to selectively remove silicate glass layer 91 from directly below non-masked region 93, which corresponds to spacing $W_2$. For the etching gas, one uses a mixture of $CF_4$, $CHF_3$ and argon, which have selectivity for polysilicon and are anisotropic. For example, one would do the etching with 8sccm of $CF_4$, 12sccm of $CHF_3$ and 150sccm of argon at a pressure of 200Torr and a power of 4.7 Watts/cm$^2$, whereby silicate glass layer 91 will be etched perpendicularly in the shape that perpendicular surface 95 has.

**0056** That is, because we fixed the size relationships of mask 92 in Figure 6 as $W_1>W_2$ and $W_2/H\leq 1/2$, the width $W_2$ of non-masked region 93 (the opening) in which glass layer 91 is etched is smaller than the width $W_1$ of the remaining part and non-masked region 93's width $W_2$ is enough smaller than its height H. So, not only is it difficult for the isotropic etching gases and their reactive radicals to penetrate narrow non-masked region 93, but also vertical-axis etching by etchant gases that are relatively anisotropic becomes dominant. As a result, as the etching progresses, laminates of polymer-like substances do not adhere to the sides of glass layer 91, and the etchant gases affect glass layer 91 only on a nearly perpendicular axis. In Figure 14 the solid arrows show the etching of glass layer 91, while the broken-line arrows show the progress on a perpendicular axis.

**0057** The above-noted aspect ratio ($W_2/H$) in this etching is fixed before etching by the ratio of the thickness (height) to the spacing of masks 92; but actually as the etching proceeds the height H becomes greater, reaching a maximum of the total of the thickness of mask 92 and glass layer 91. Here, one can do this to $W_2$ = 0.2$\mu$, H = 2.0$\mu$m and glass layer 91's thickness at about 1.0$\mu$m, so that one may make $W_2/H$ a minimum of around 1/16 (when one considers the above-noted total amount) and a maximum of 1/2 (before etching). If this $W_2/H$ is greater than 1/2, perpendicular etching qualities of glass layer 91 become poor; and when less than 1/16, etching failures readily arise. This $W_2/H$ moreover can yield critical effect results in the range of 1/5 ~ 1/2.

**0058** Now, as shown in Figure 8, one removes masks 92 and uses CVD to form polysilicon layer 96 which will be the capacitors' lower electrodes and then—as shown in Figure 9—uniformly

etches polysilicon layer 96. At this point, if underlying polysilicon layer 11 is not etched away before depositing polysilicon layer 96, this polysilicon layer 11 also will be etched. Also, one leaves polysilicon layer 96 on the sides of spacers 91. For this etching, one uses chlorine gas with its superior anisotropy and so its lowered selectivity ratio toward oxides. So, for example, one does anisotropic etching of polysilicon layer 96 at 40sccm of chlorine, a pressure of 5mTorr and a power of 180mA. In this case, since the sidewalls of spacers 91 are perpendicular, polysilicon layer 96 will be uniformly etched perpendicular to the substrate, i.e., from effects at right angles to the substrate and it will remain with sufficient thickness on the side surfaces of spacers 91.

**0059** Now spacer material 91, which supports the sides of polysilicon 96, are etched away by wet-etching, as shown in Figure 10, for instance with fluoric acid or buffered fluoric acid which is selective toward polysilicon, thus forming tubular polysilicon lower electrode 96 connected to substrate 1's $N^+$ region 3.

**0060** As shown in Figures 11 and 12, with CVD over all surfaces one laminates, respectively, silicon nitride film 77, which is highly dielectric, and the polysilicon capacitor's upper electrode 78 (plate electrode) to fabricate memory cells MC in a COB structure having multiple stack-cell capacitors CAP. Insulating layer 97 is further added onto these memory cells, as shown in Figure 13.

**0061** As noted above, the memory cells of the dynamic RAM from this application example—as was shown in their fabrication processes noted above—have their capacitors' lower electrodes 96 with inner diameters matching the diameter $W_1$ for masks 92 discussed with Figure 6, and spaces between adjoining capacitors' lower electrodes 96 that match adjoining spacing $W_2$. As lower electrodes 96 have a vertical tubular shapes, one can narrow the spacing between adjoining capacitors so as to improve the degree of integration.

**0062** Again, because the etchant gas that causes laminates to form can scarcely penetrate the above-noted spaces that correspond to the regions 93 not masked by mask 92 that is used for patterning spacers 91 that set the shape of the lower electrodes during fabrication, vertical anisotropic etching can be done well on a perpendicular axis. So, one can keep the lower electrode's thickness sufficient after etch-back and

so achieve that perpendicular shape. I.e., as radicals from the etchant gases can scarcely penetrate non-masked region 93, one can give full play to vertical anisotropic etching. Thus, one can get good perpendicularity for the sides of spacer material 91, prevent lateral etching when doing the etching of polysilicon layer 96 that will be the capacitors' lower electrodes and so can sustain their thickness.

**0063** As a result, having prevented film thinning as already discussed, one need not pre-thicken the configuring material layer of the lower electrodes, and can make spacing between capacitors as narrow as possible and so devise the devices' higher density and improve their degree of integration.

**0064** From the above-noted etch-back, polysilicon film 96 gets vertical surfaces from the bottom of its inner surfaces to their top; but its outer surface is vertical from the lower end to a point part way up its side, and from there the film gradually thins.

**0065** Also, to compensate for the fact that the height of polysilicon layer 96 will be reduced by the etch-back, spacer material 91 is made higher in advance so that one can keep it high enough after the etch-back. By doing the etch-back on the perpendicular axis adequately, the polysilicon that would tend to remain on the stepped portions of the semiconductor substrate is totally removed at the same time, enabling one to prevent short-circuiting or the like between elements due to leftover polysilicon.

**0066** In Figure 15 we used narrowly spaced ($W_2$) mask 92 and widely spaced mask 72 to roughly compare the shapes of glass layer 91, which is the spacer material, with layer 71 after etching. Whereas the former yields a perpendicular surface 95, the latter became a sloped surface and the dimensions of its spacer material become larger.

**0067** In Figure 16, when one sets the above-noted aspect ratio of mask 92 as in this application example ($W_2/H \geq 1/2$) and improves the anisotropy of the etchant gas at the same time (e.g., by reducing the flow of $CHF_3$), one can reduce widening of the spacer material after etching at the spacing width ($W_2$) of mask 92 as in (A) and greatly improve the vertical etching traits. (B) in the figure shows the case where the above-noted etchant gases' anisotropy alone was improved; and widening of the spacer material's dimensions was constrained more than with the usual method. (C) in the figure shows a

case of the usual method (when neither of countermeasures (A) or (B) was done). The etching qualities were improved to some extent.

**0068** That is, with the usual fabricating method wherein the anisotropy is not improved, there is considerable increase in the remaining spacer material's dimensions for the mask pattern spacing. This is thought to be because there is a high ratio of polymers from the etching gases adhering to the sidewalls of the etched oxide film, which increases the films' width. However, if one uses an etching process that improves anisotropy by cutting, for instance, the ratio at which $CHF_3$ is mixed in, one can suppress the enlargement of films overall. Also, one can greatly restrain widening of oxide films by narrowing the spacing of the mask pattern or by increasing the height of the oxide film.

**0069** As shown in the enlarged diagram of Figure 17, the etch-back of polysilicon layer 96 creates polymer laminates 79 on the inner surface at the top of polysilicon layer 96, as discussed already in connection with Figure 36, while natural oxide film 80 easily forms on its outer surface. It is desirable to remove these by some method, such as etching.

**0070** Figures 18~24 show a second application example of applying this invention to a dynamic RAM.

**0071** To explain the dynamic RAM of this application example along with its fabrication processes, one first makes a contact hole in insulating layers 6 and 7 on source region 3 in the memory area, just as in the first application example illustrated in Figures 1~3, and then—as shown in Figure 18—applies silicate glass layer 91 by CVD to the entire surface, including the contact hole.

**0072** This glass layer 91 will become a support (or a spacer for fixing the shape of the polysilicon lower electrode) when forming the tubular (crown-shaped) polysilicon lower electrode of the stacked-cell capacitors described later. It is made, e.g., about 5000Å thick. This silicate glass-insulating layer 91 consists of a non-doped silicate glass without impurities. (However, one may dope it with an impurity depending on the type and concentration.)

**0073** Then one forms, in a prescribed pattern, photo-resist masks 102 for etching this insulating layer 91 into the spacer

shapes. With these masks 102, one makes the diameter of the masks $W_1'$, the spacing between each $W_2'$ and their thickness H'. So then one a least has $W_1' \leq W_2'$ and desirably ratios of $1XW_1' < W_2' \leq 10W_1'$, $W_2'/H' \leq 1$ (also $2 \leq W_2'/H' \leq 8$). For instance, it is good to make the masks' $W_1'$=0.2~0.3μm, $W_2'$=0.6~1.2μm and H' = 0.7~1.0μm, with $W_2'/H'$ at 1.5, for instance.

**0074** As shown in Figure 19, one then uses masks 102 to etch insulating layer 91, selectively removing silicate glass layer 91 from directly under non-masked region 103, which corresponds to the outer diameter of the capacitors' lower electrodes. For the etchant gas in this dry etching one uses a mixture of $CF_4$, $CHF_3$ and argon, which are anisotropic and selective for polysilicon. For instance, one does the etching with 5sccm of $CF_4$, 15sccm of $CHF_3$ and 200sccm of argon at 400Torr pressure and power at 4.7W/cm². As the figure shows, silicate-glass layer 91 will be etched into shapes with sloped surfaces 74.

**0075** I.e., because in Figure 18 we set the size relationships at $W_1' << W_2'$ and $W_2'/H' \leq 1$, the width $W_2'$ of non-masked region 103 (the opening) where glass layer 91 is etched is much larger than the diameter $W_1'$ of the part remaining. So, the isotropic etchant gases easily get into wide non-masked region 103 and their reactive radicals easily penetrate, while etching also occurs on a perpendicular axis due to anisotropic etchant gases. The result is that polymer laminates adhere to the sides of glass layer 91 as the etching progresses and the etchant gases can scarcely affect glass layer 91 on the perpendicular axis.

**0076** So, because here mask 102 is given a pattern the reverse of that discussed in Figure 7's first application example, by making mask 102's opening wide, the sides of spacer material 91 do not become perpendicular, just as in the usual case, but are sloped, making it basically different in that spacer 91's etched part is—as noted below—made the region for the capacitor's lower electrode.

**0077** As in Figure 20, mask 102 is removed and polysilicon layer 106 is applied by CVD to the entire surface including contact hole 10.

**0078** Now, as shown in Figure 21, one fills photo resist 101 into depression 10 between adjoining spacer materials 91–91 to which polysilicon layer 106 has been applied to a depth below the upper surface of spacer material 102.

**0079** Then, as shown in Figure 22, one uses photo resist 101 as a mask to etch-back polysilicon layer 106 where it is exposed in the non-masked regions. For this etch-back, one uses chlorine gas for its superior anisotropy and lowered selective ratio with oxides, doing anisotropic etching of polysilicon layer 106 with, for instance, 40sccm of chlorine at 5mTorr pressure and 180mA power. In this case, polysilicon layer 106 is easily thinned by the etch-back; but since it is protected by resist 101 on the sides of spacer material 91, its thickness will be sufficiently preserved after the etch-back.

**0080** As shown in Figure 23, one now removes resist 101 and uses wet etching, such as with fluoric acid (or buffered fluoric acid) for its selectivity with polysilicon, to remove spacers 91 that support polysilicon 106 on its sides and so form tubular polysilicon lower electrode 106, which is connected to substrate 1's $N^+$-type region 3.

**0081** Next, as shown in Figure 24, one respectively laminates over the entire surface by CVD highly dielectric silicon nitride film 77 and polysilicon upper electrode 78 (plate electrode) to fabricate memory cell MC with multiple stack-cell capacitors separated from each other.

**0082** As noted above, the dynamic RAM memory cells from this application example have, as indicated in its manufacturing process, outer diameters for capacitor lower electrodes 106 matched to the diameter $W_2'$ of the non-masked regions for masks 102 discussed under Figure 18, and spaces between adjoining capacitor lower electrodes 106–106 that match spacing $W_1'$. So, even with lower electrodes 106 having the crown shape of an inverted base, one can make the spaces between adjoining capacitors narrow and improve integration.

**0083** Also, even if etchant gases—the cause of laminate formation—should penetrate and etch spacer material 91 at a slant in the above-noted diameter $W_2'$ that matches the non-masked region 93 of mask 92 used in patterning spacer material 91, which in turn defines the shape of lower electrodes 106 during fabrication, during polysilicon layer 106's etch-back one can use resist 101 to keep polysilicon layer 106 on the sides of spacer material 91 from being etched and so protect its thickness.

**0084** This results in preventing film thinning, as already discussed, and eliminates the need for pre-thickening the configuring material layer of the lower electrode and enables one to narrow the spacing between capacitors to the extent possible. That enables one to work out high density of the device and improve its degree of integration.

**0085** Polysilicon layer 106 has flat side surfaces from top to bottom, but its inner surface is flat from the bottom to a point part way up, and from there the film gradually thins.

**0086** Figure 25 shows the third example of applying this invention to a dynamic RAM.

**0087** In the process of fabricating a dynamic RAM with this application example the process that differs from the above-described examples is that of preventing the creation of valleys that tend to occur at the top of the polysilicon layer during etch-back of the polysilicon that will be the above-discussed capacitors' lower electrode.

**0088** That is, as shown in Figure 25(A), after using CVD to apply polysilicon layer 96 onto spacer material 91, if one proceeds with the etch-back of polysilicon layer 96, the above-described polymer-like laminate 79 and natural oxide 80 will easily form at its top. The polysilicon valleys caused by these sometimes have a height of about 800Å.

**0089** So, as a condition for the polysilicon layer 96's etch-back, one does the etch-back using etchant gases having only slight amounts of etchant components that are isotropic and so reduce the selectivity toward oxide film; and that can prevent the creation of valley shapes.

**0090** Concretely, one uses chlorine for the etchant gas without using oxygen because that lowers selectivity toward oxide film. With a mixture of chlorine and oxygen the relative etching rate is about 50:1 for polysilicon:oxide, while with chlorine alone the rate is about 20:1, enabling one adequately to do perpendicular etching of the polysilicon and also to etch oxides. Again, it is good to admix $SF_6$ as an isotropic component. Consequently, in this application example, one instance of etchant gases used for the etch-back is a mixture of 40sccm of chlorine and 4sccm of silicon fluoride, etching at a pressure of 5mTorr and power of 200mA.

**0091** This way, during etching one can sufficiently etch polysilicon film 96 and also the polymer-like laminates (mainly polymerized silicons) that cause the valleys and the natural oxide films (and also just a little bit of the top of spacer material 91). As a result, as shown in Figure 25(C), polysilicon film 96 will be free of valleys and 800Å or more of region A will be removed from the top surface of spacer material 91, lwaving a perpendicular shape for the sides of spacer material 91 with only a slight thickness reduction.

**0092** So, as discussed with Figures 11 and 12, when applying dielectric film 77 one can get good film adhesion and quality and improve voltage resistance. Moreover, because one can avoid valley formation during the etch-back, no additional process to remove valleys is needed and one can make capacitors that meet the goals with a minimum of processes.

**0093** The processes of this application example should be applied also to the first and second application examples, and may be applied, too, to other manufacturing processes.

**0094** Figures 26 and 27 show the fourth application example of applying this invention to a dynamic RAM.

**0095** The fabrication process of the dynamic RAM from this application example differs from the above-noted third application example in that after the etch-back it removes the valleys created on top of the polysilicon layer that will be the capacitors' lower electrode.

**0096** I.e., after the etch-back process of polysilicon layer 96 illustrated in Figure 9, when valleys remain as noted above in the top part of polysilicon layer 96, one does isotropic polysilicon etching at 1.4Torr and 350W, using, for instance, 400sccm of oxygen and 30sccm of $CHF_3$ as etchant gases at an etch rate of 100Å/min to remove the valleys. That enables one to make the shape shown in Figure 25(c).

**0097** When the valley projections are removed by such an after-processing step, because one transports the etchant gas and places it in a processing chamber, one can use the equipment shown in Figure 26. I.e., one passes high-frequency voltage 112 between paired electrodes 110-111 to create ions (radicals) of etchant gases 113, introducing only radicals 114 into chamber 115 over substrate 1 to do isotropic etching. Anisotropic processing with ions having directionality is not done.

**0098** Also, because this after-processing is incompatible with etching oxide layers and polysilicon layers or with the process of depositing polysilicon, these processes are added on in their own processing chambers; and one should install a chamber for this after-processing to round (remove) the valley projections. The reason is because that allows one to do the processing continuously without changing the processing steps or breaking the vacuum. Figure 27 shows a sketch of the layout that enables one to use chamber 115 for that after-processing sequentially with the chamber for the processing of the prior stages.

**0099** It is desirable also to apply the steps of this application example to the above-described first or second application examples, and it may also be applied to other manufacturing processes.

**0100** The foregoing has explained this invention's application examples; however the above-described application examples can be further altered based on the technical concepts of the main invention.

**0101** For instance, the sequences and combinations of the above-described processes, as well as the kinds of etchant gases can be variously altered; or one can change the substances used or the patterns. In particular, instead of using polysilicon with its large crystals as the material for the capacitors' lower electrodes, one may use amorphous silicon. In some cases amorphous silicon would be advantageous for making perpendicular shapes. Or, that shape may be round concentric tubes.

**0102** Again, with the above-described second application example, there is no particular requirement for selectivity and anisotropy for the etchant gases for the dielectric or polysilicon layers. In the above-described second and third application examples the capacitors need not necessarily be aligned in multiples.

**0103** In each of the above application examples we described memory cells of a COB structure; but this invention of course can be applied to memory cells of CUB structure (cell under bitline). In addition, the conductive types of the above-described semiconductor regions can be switched. And, this invention can also be applied to other semiconductor memories and other devices.

**0104 Effects of Adopting This Invention** As discussed above, this invention is one in which multiple stack-cell capacitors are aligned with prescribed spacing on a semiconductor substrate, and each consists of a nearly perpendicular tubular lower electrode, a dielectric film and an upper electrode, with the afore-noted spacing on their axis of alignment being smaller than the inner diameter of the afore-noted lower electrodes, so that one can narrow the space between capacitors and so improve integration. Also, since it is difficult for etchant gases—a cause of laminate formation—to penetrate the above-noted spaces corresponding to regions not masked by the mask used in patterning the spacer material which defines the shape of the of the lower electrodes during fabrication, and since this enables one to do perpendicular anisotropic etching on the vertical axis, one can make the thickness of the capacitors' lower electrodes adequately great to sustain their perpendicular shape.

**0105** Again, because the stack-cell capacitors are installed on a semiconductor substrate and consist of a lower electrode shaped in cross section like an inverted base, a dielectric film and upper electrode, and their lower electrodes are installed on the non-masked region corresponding to the spacing between the lower electrodes that adjoin the spacer material, and the spacer material is removed at the same time, one can get lower electrodes in the above-stated shape.

Hence, having lower electrodes of such a shape enables one to narrow the spacing between adjoining lower electrodes, which makes possible devices of higher density and greater integration.

**0106** In making lower electrodes of an inverted base shape in this case, because the spacer material is etched via the above-noted first masking material's non-masked region, the side surfaces of the spacer material have become sloped after etching due to the adhesion of laminates. But, here the configuring material layer applied for the lower electrodes is protected by the 2$^{nd}$ masking material up to the spacer material's upper surface position and so is not etched. So, the remaining lower electrode is sufficiently thick that one can provide the inverted base shape matching the above-noted spacer material's slanted surface. Thereby, for the lower electrodes (i.e., the etched part of the above-noted spacer material), spaces can be made small between adjoining lower

electrodes, enabling the capacitors to become high density and highly integrated.

**0107** Also, at the time of the lower electrodes' configuring material layer's etch-back, etching is done under conditions of lowered etching selectivity ratios for oxides and isotropic etching components. So, etching is done so as not to create the natural oxides or polymer-like laminates that tend to arise on the outer and inner surfaces of the configuring material layer of the lower electrodes. So, one can eliminate the occurrence of valleys. Consequently, one can form good quality and adequately thick dielectric films on the lower electrodes, avoid insulating failures and improve voltage resistance, raising the reliability.

**0108** Furthermore, after etch-back of the lower electrodes' configuring material, one removes valleys on top of it by isotropic etching and so can form lower electrodes without valleys while preserving the thickness and quality of the dielectric films. Moreover, even if one adds a process that removes the valleys, this can easily be done by transfer to a separate processing chamber while sustaining the vacuum.

**Simple Explanation of Figures**

**Figure 1** is an enlarged cross-sectional diagram of one processing stage of the dynamic RAM fabrication method from the first application example of this invention.

**Figures 2~14** each are enlarged cross-sectional diagrams of other processing stages of the same fabrication method.

**Figure 15** is a sketched cross-sectional diagram illustrating a comparison of one processing stage of the same fabricating process.

**Figure 16** is a diagram showing a comparison of dimensions after etching in one processing stage of the same fabricating process.

**Figure 17** is a cross-sectional diagram showing a greater enlargement of the main parts in one processing stage of the same fabricating process.

**Figure 18** is an enlarged cross-sectional diagram of one processing stage of this invention's second application example for a dynamic RAM's fabricating process.

**Figures 19~24** each are enlarged cross-sectional diagrams of other processing stages of the same fabricating process.

**Figure 25** is enlarged cross-sectional diagrams of the main processing stages for the fabrication process of a dynamic RAM from the third application example of this invention.

**Figure 26** is a sketched cross-sectional diagram of a device used in fabricating a dynamic RAM with the fourth application example of this invention.

**Figure 27** is a sketched layout of another device used in fabricating the same dynamic RAM.

**Figure 28** is an enlarged cross-sectional diagram of one processing stage in the usual method of dynamic RAM manufacture.

**Figures 29~32** are enlarged cross-sectional diagrams of other processing stages in the same manufacturing method.

**Figures 33~36** are enlarged cross-sectional diagrams of the processing stages in the same manufacturing method.

**Explanation of Keying Symbols**

| | |
|---|---|
| 1 . . . . . | Silicon substrate |
| 2 . . . . . | $SiO_2$ film |
| 3 . . . . . | $N^+$ source region |
| 4 . . . . . | $N^+$ drain region |
| 5 . . . . . | Gate oxide film |
| 6,7,61,70,97 . | Insulating layers |
| 10 . . . . . | Contact hole |
| 11,76,96,106 . | Polysilicon layer (lower electrode) |
| 60 . . . . . | Silicon nitride sidewall |
| 62 . . . . . | Sidewall |
| 71 . . . . . | Oxide or silicate-glass spacer |
| 72 . . . . . | Photo-resist mask |
| 74 . . . . . | Sloped surface |
| 77 . . . . . | Dielectric film |
| 78 . . . . . | Polysilicon layer (upper electrode) |
| 79 . . . . . | Polymer-like laminate |
| 80 . . . . . | Oxide |
| 91 . . . . . | Silicate glass layer (insulating layer) |
| 92, 102 . . . | Mask |
| 93,103 . . . . | Non-masked region |

95 . . . . . Perpendicular surface
101 . . . . . Resist
$W_1$ . . . . . Diameter
$W_2$ . . . . . Spacing
H . . . . . Height or thickness
WL . . . . . Word line
BL . . . . . Bit line
CAP . . . . . Stack-cell capacitor
MC . . . . . Memory cell

[Figure 15]
[left top] Narrow space width
[right top] Wide space width

[Figure 16]
[vertical axis] Dimensional swelling
[lateral axis] Spacing width
A: Measures to improve anisotropy + aspect ratio enlargement
B: Measures to improve anisotropy
C: Usual method

[Figure 27]
[Clockwise from lower left]
Chamber for oxide film etching
Chamber for polysilicon etch-back
Chamber 115 for after-processing
Chamber for polysilicon or amorphous silicon deposition

[Translator's note: text items following the figures, already incorporated in the page 1 header, list the additional inventors.]